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(54) Substrate bias generator

(57) A substrate bias generator for CMOS semiconductor circuitry comprises a charge pump (10) arranged to receive four oscillating signals (V14, V24, V34 and V46) and to develop at its output (12) a substrate bias voltage (VBB). All of the transistors in the charge pump circuit are P channel.

The voltage at a first node (18) is arranged to follow the voltage of a first oscillating signal V14 applied to a first input (14). In addition, the first node (18) is periodically grounded by way of a transistor (20) controlled by a second oscillating signal (V24) coupled to its gate. The first node (18) is selectively coupled to the output (12) by way of a transistor (42) controlled by a third oscillating signal (V34) coupled to its gate such that a negative voltage is developed at the output (12).

FIG. 1

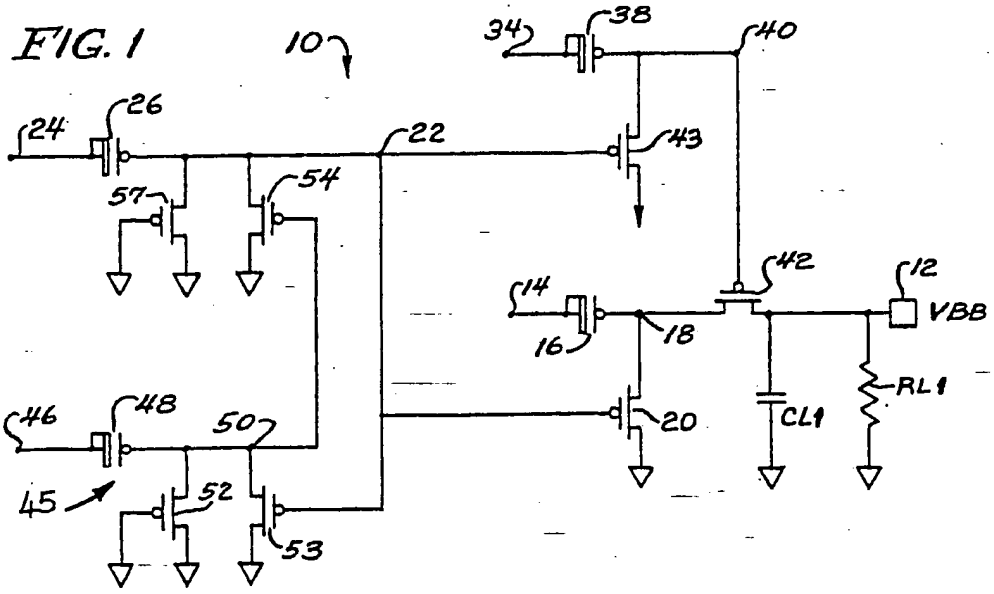

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FIG. 1

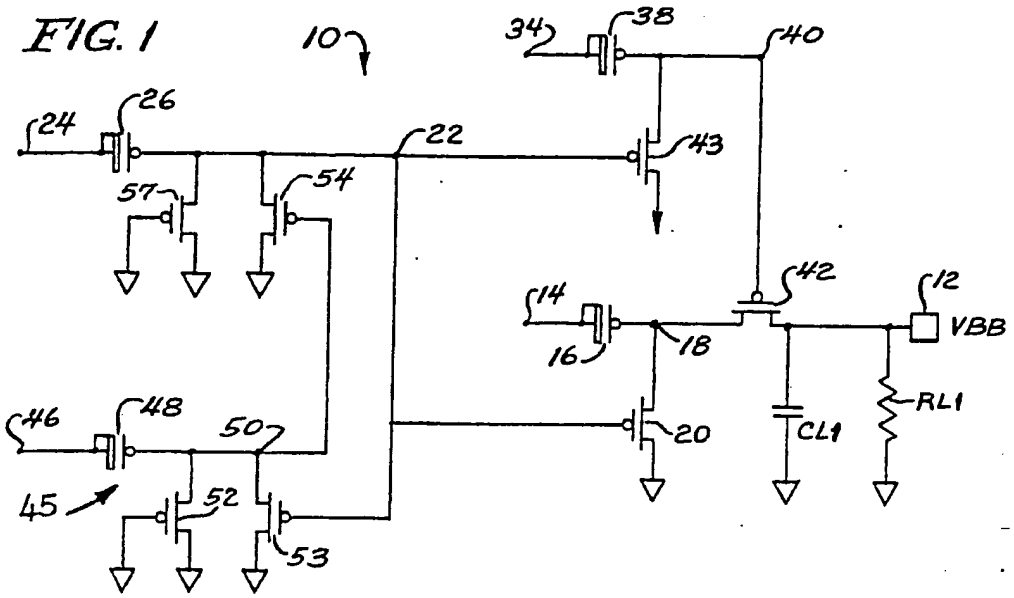


FIG. 2

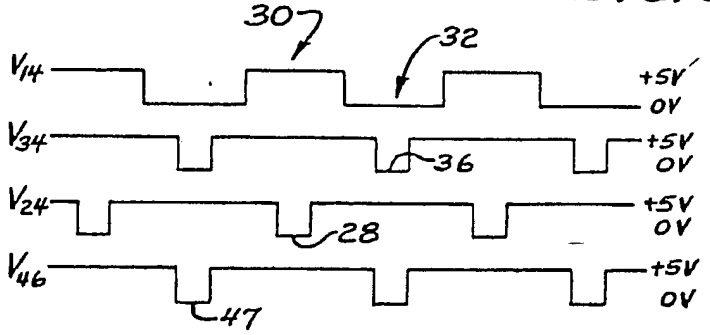
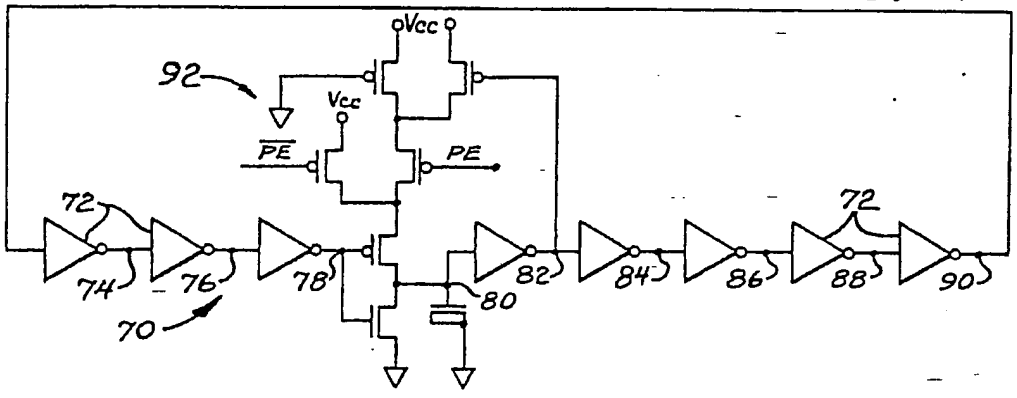


FIG. 4A



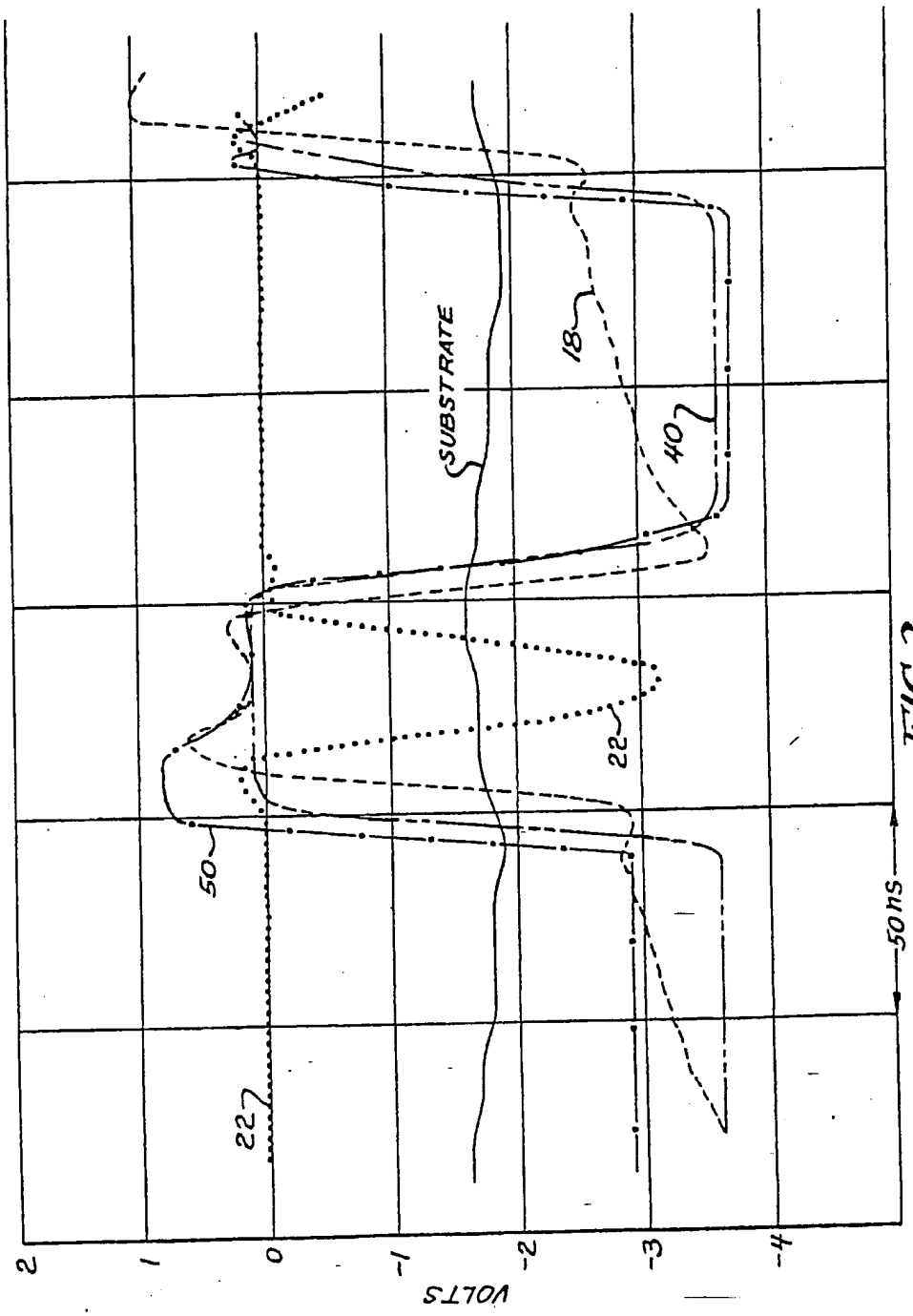


FIG. 3

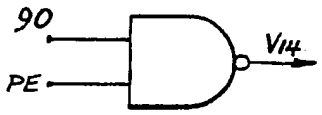


FIG. 4B

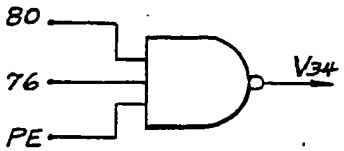


FIG. 4C

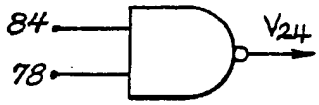


FIG. 4D

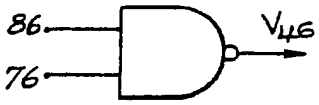


FIG. 4E

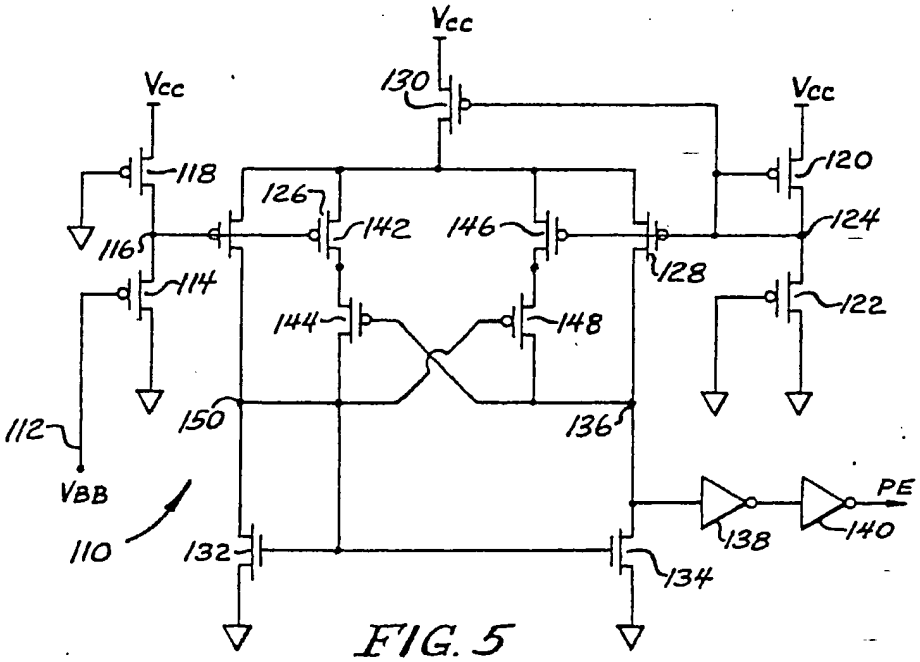


FIG. 5

SPECIFICATION

Substrate bias generator

The present invention relates to a substrate bias generator for CMOS semiconductor circuitry.

A substrate bias on a CMOS circuit gives better control over thresholds, improves the speed of the circuitry, and guards against negative gliches to control latch-up.

According to one aspect of the present invention there is provided a substrate bias generator for developing a substrate bias voltage, said generator comprising first input means for receiving a first oscillating signal, said first input means being coupled to a first node; first selectively operable means for clamping said first node to a reference level, and means for coupling said first node to an output.

According to a further aspect of the invention there is provided a CMOS substrate bias generator comprising a generator circuit for developing a substrate bias voltage, and a regulator for controlling the operation of said generator circuit, said regulator including an input circuit coupled to receive a VBB signal representative of the substrate bias voltage, a reference circuit providing a reference voltage, a comparison circuit coupled to said input circuit and to said reference circuit for comparing voltage levels therein, and output means responsively coupled to said comparison circuit for providing a signal to said generator circuit.

Preferably, the substrate bias generator uses only P channel transistors in the charge pump thereof. This minimizes electron injection from nodes which swing to a negative voltage. Such electron injection can cause loss of capacitively stored data in a dynamic RAM, for example, which can be sensitive to this.

A substrate bias generator of the invention can be used in any CMOS memory circuit or CMOS micro-processor circuit which uses N channel transistors operating with a negative substrate.

In an embodiment of this invention, a regulator circuit for a CMOS charge pump is provided and includes an input circuit, a reference circuit, a comparator between them, and a hysteresis circuit regulator. Circuitry is also provided so that first order effects are eliminated.

An embodiment of the present invention will hereinafter be described, by way of example, with reference to the accompanying drawings wherein like reference numerals designate like elements, and in which:

Figure 1 schematically illustrates a CMOS charge pump of the invention;

Figure 2 shows a set of waveforms received by the circuit of Figure 1;

Figure 3 is a set of waveforms to show the operation of the circuit of Figure 1,

Figure 4 shows a set of circuits for generating the input signals to the charge pump circuit of Figure 1; and

Figure 5 schematically shows a regulator circuit for use in combination with the charge pump shown in Figure 1.

In the Figures, a P channel device is signified by a small circle attached to the gate of a transistor.

A. The Charge Pump

The accompanying Figures illustrate embodiments of circuits of the present invention together with waveforms which are useful in comprehending the operation of the circuits. Figure 1 schematically illustrates the circuit 10 of a charge pump for a substrate bias generator. It will be seen that the circuit 10 includes transistors which are only P channel. Four oscillating input signals, whose waveforms are illustrated in Figure 2, are applied to the circuit 10 which is arranged to provide a VBB signal at its output 12. In describing circuit 10, reference will be made to various elements thereof together with reference to the waveforms illustrated in Figure 2.

An input 14 of the circuit 10 receives a waveform V14 which, by way of example, is a square wave oscillating between 0 volts and +5 volts (VCC) and having a 50% duty cycle. The waveform V14 is applied to a capacitor 16, and the voltage at a node 18 on the other side of the capacitor 16 follows the waveform V14. It is intended that node 18 should be between 0 volts and −VCC (−5 volts). At a time when the waveform V14 is at 5 volts, the node 18 is clamped to ground via the source-drain path of a transistor 20 whose resistance when ON may be as low as twenty ohms.

The gate of the transistor 20 is coupled to a node 22. An input 24 of the circuit 10 receives a waveform V24 and capacitively couples this waveform to node 22 by way of a capacitor 26. Thus, the voltage at node 22 follows the waveform V24.

The waveform V24 contains a portion 28 at 0 volts. The voltage at node 22 is caused to drop to -5 volts during the portion 28 of the waveform V24. As can be seen in Figure 2, this occurs when the waveform V14 is at a positive level 30. As a result of the timing of the waveform V24, and specifically of its portion 28, transistor 20 turns ON to clamp the node 18 to ground. Then, when waveform V14 goes from +5 volts to 0 volts, as shown at portion 32, node 18 corresondingly will be driven down from 0 volts to −5 volts.

The node 18 is selectively coupled to the output 12. During portion 32 of the waveform V14, another waveform V34, which is applied to an input 34 of the circuit 10, also drops to 0 volts as shown at 36. Waveform V34 is coupled by a capacitor 38 to a node 40 which is coupled to the gate of a P channel transitor 42. The source-drain path of the

transistor 42 couples the negative 5 volts at node 18 to the output 12. Because of the very large capacity of the substrate, VBB at the output 12 will drop only a small amount. Eventually, VBB will reach approximately −VCC/2.

It will be understood that the voltage at node 40 will be caused to vary in steady state operation between −5 volts and 0 volts as a result of the clamping effect of a transistor 43, whose gate is controlled by the voltage at node 22. Due to the phase separation between waveforms V24 and V34, node 40 will be clamped to ground at times when V34 is high, and when V34 drops low, that will drive node 40 negative by a voltage swing of five volts, in much the same manner as the operation of other nodes discussed herein and shown in the charge pump 10.

In operation, waveform V24 starts at VCC. When it drops to 0 volts, the voltage at node 22 drops negative and this turns on the transistor 20. During this voltage drop, waveform V14 is high, and so node 18 is at its own highest voltage. Accordingly, as a result of the transition to 0 volts in waveform V24, node 18 is grounded. It will be released when V24 goes high. Shortly thereafter, waveform V14 drops from VCC down to 0 volts as a result of portion 32 in waveform V14. This drives node 18 to -VCC. Next, this negative voltage is coupled to output 12 as a result of a portion 36 of waveform V34. Thus, waveforms V14, V24 and V34 are applied in the circuit 10 to develop a negative voltage at the output 12.

Those skilled in the art will appreciate that the transistors 20 and 42 will both be OFF when a transition occurs on waveform V14. This promotes speed. It will also be appreciated that while node 18 is low, a signal gates the transistor 42 to couple node 18 to the output 12. In this embodiment, a low going portion of waveform V34 is used advantageously for this, although other circuitry can be substituted. Moreover, it will be appreciated that when node 18 is high, a signal is used to cause clamping to ground. In particular, this is a low going portion of the waveform V24, although substitutions can be made.

The circuit 10 includes further elements which are shown in Figure 1 and which perform a standby or initialization function. It will be understood that when VBB achieves a certain level, the charge pump 10 will stop pumping. If VBB rises, a standby circuit 45 is provided to ensure that the pump 10 will be ready for use. This is done by ensuring that nodes 18 and 22 are at ground potential. The standby circuit 45 comprises an input 46 which receives a waveform V46. The waveform V46 is illustrated in Figure 2 and includes a portion 47 at zero volts. The standby circuit also comprises a capacitor 48 which couples the input 46 to a node 50. When oscillations start in waveform V46 during power-up, a transitor 52 clamps the capacitor 48 to a P channel threshold voltage. During such power-up, the clamp has to be at a P channel threshold, and after power-up, the clamp can be to ground.

After power-up, node 50 is coupled selectively to ground by the source-drain path of a transistor 53 whose gate is controlled by the signal at node 22. There is a phase difference between the signals V24 and V46 applied to inputs 24 and 46, respectively, and this phase difference causes the transistor 53 to clamp node 50 to ground at some time. Thereafter, due to the timing of portion 47, the voltage at node 50 will be driven negative when the clamp (transistor 53) is released.

At some time when node 22 is high, the voltage at node 50 will drop to negative, and a transistor 54 will turn ON because its gate is coupled to node 50. This clamps node 22 to ground, in the manner discussed already, whereby the voltage range at node 22 will be between 0 volts and −5 volts, instead of, for example between −3 volts and +2 volts (because if the voltage at node 22 goes to a positive potential, it will be coupled to ground by the source-drain path of the transistor 54). Similarly, the voltage at node 50 is kept between 0 volts and −5 volts through the action of the transistor 53.

It should be mentioned that the source-drain path of a transistor 57 couples node 22 to ground. The gate of the transistor 57 is grounded. During power-up, when oscillations shown in waveform V14 commence, the transistor 57 clamps capacitor 26 to a positive excursion of the magnitude of VTP, which is a P channel threshold of about 1.5 volts.

Also shown in the circuit 10 illustrated in Figure 1 are a capacitance CL1 and a resistance RL1. These are representative of the substrate.

It will be noted that all of the nodes of the charge pump are located inside N wells and are not connected to the substrate or to N channel transistors. Hence none of these nodes can inject electrons into the substrate. This prevents loss of signal from capacitively charged nodes.

The capacitors 16, 26, 38 and 48 can be P channel devices, but they are preferably N channel depletion types. This has the advantage of preventing substrate bouncing with the well voltages. The use of N channel devices here is acceptable because no N diffusions go negative in the circuit 10 shown in Figure 1.

B The Input Signal Generators

The waveforms V14, V24, V34 and V46 are generated in circuits schematically illustrated in Figure 4 which shows a collection of schematic circuit diagrams. The basic element of Figure 4 is illustratively shown in Figure 4A and includes a ring oscillator 70 having eight

stages of inverters 72 connected in series to form nine nodes 74, 76, 78, 80, 82, 84, 86, 88 and 90. Such circuits are known and those skilled in the art who need no further explanation to construct the oscillator circuit 70. Suffice it to say that the voltages between adjacent nodes in the ring oscillator circuit 70 are cyclic and have a phase separation.

Further circuitry 92 is provided between node 78 and, for the most part, node 80, although one gate is coupled to node 82. Circuitry 92 is used to slow the frequency when the bias generator is not pumping, that is, when the pump enable signal PE is 0. This technique is known in the art and needs no further explanation. The PE signal is developed in a regulator circuit described hereinbelow.

The waveforms V14, V24, V34 and V46, which are coupled respectively to inputs 14, 24, 34 and 46 (Fig. 1), are generated in the circuits of Figures 4B, 4C, 4D and 4E. These are all NAND circuits coupled to the pump enable signal PE and to the nodes of circuit 70. The NAND circuits avoid ever having floating nodes.

From considering Figure 4, it will be understood that when the pump enable signal is off (at 0 volts), voltages V14 and V34 are stable at VCC, whereas waveforms V24 and V46 oscillate as shown in Figure 2.

C. The Regulator Circuit

The pump enable signal PE is generated by a regulator circuit 110 shown in Figure 5. It will be seen that this regulator circuit has a pair of nodes on opposing sides of a differential amplifier which is modified to include hysteresis circuitry. Circuit 110 seeks to regulate the substrate voltage VBB to −VCC/2 which is about −2.5 volts.

Starting at the left side of the diagram of circuit 110 it will be seen that the circuit has an input 112 to which the substrate voltage VBB is applied. The input 112 is connected to the gate of a transistor 114. A node 116 is formed at the junction of the source of the transistor 114 and the drain of another transistor 118, whose gate is grounded. Both transistors 114 and 118 are P channel transistors, as are most of the transistors in the circuit 110. The voltage at node 116 will naturally go to VCC/2 and hence the bias on the transistors 114 and 118 will be equal. When node 116 is at VCC/2 the transistors 114 and 118 will both be ON because their drain to source potentials are −VCC/2 and their gate to source potentials are both −VCC. As VBB goes more negative, the gate to source potential of the transistor 114 increases, and node 116 moves towards ground. This method of sensing VBB does not draw any current from the substrate.

At the right side of the diagram of the circuit 110, a pair of transistors 120 and 122 have their source-drain paths connected in series to couple VCC to ground. A node 124 is located between the two transistors 120 and 122. Both the transistors 120 and 122 are ON; the drain to source potential of each is −VCC/2 and the gate to source potential of each is also −VCC/2. Thus, unlike node 116 which is dependent on VBB being negative, the voltage at node 124 is independent of VBB. Node 124 is therefore always at a voltage of VCC/2.

The middle portion of the diagram of the circuit 110 in general compares the voltage at node 116 with the voltage at node 124 and generates the pump enable signal PE as a result of this comparison. If the VBB voltage is greater than −VCC/2, then node 116 will have a voltage greater then that at node 124. On the other hand, if VBB is smaller then −VCC/2, then node 116 will have a (positive) voltage smaller than that at node 124. This middle part of the schematic diagram includes a CMOS differential amplifier formed between nodes 116 and 124. The differential amplifier includes transistors 126, 128, 130, 132 and 134. The transistors 132 and 134 are N channel transistors, whilst all of the other transistors have P channels. The gate of transistor 130 is coupled to node 124 which is always at VCC/2 or substantially +2.5 volts. Thus, the current through the transistor 130 should be generally constant. The current through the transistor 132 plus the current through the transistor 134 should always equal the current through the transistor 130. The current through the transistor 132 is affected by the voltage on the transistor 126, which is a function of VBB. Similarly, the current through the transistor 134 is affected by the voltage on the transistor 128, which generally is not a function of VBB.

Because of the differential amplifier, a small voltage difference between nodes 116 and 124 will cause a large difference in the current between the transistors 126 and 128. This current variation causes a voltage variation at a node 136. A pair of inverters 138 and 140 connected in series are coupled to the node 136. The output of the inverter 140 is the pump enable signal PE. Thus, in respect of the elements described so far, when VBB is high, higher than −VCC/2, the signal PE goes high.

The circuit 110 also includes transistors 142, 144, 146 and 148 which are arranged to add hysteresis. This will require a larger change in VBB in order to turn on the pump enable signal PE. Thus, if the voltage at node 136 is high, and the voltage at a corresponding node 150 is lower than the voltage at node 136, then transistor 148 will turn ON. The transistor 146 is always ON, so that when the transistor 148 turns ON, it helps node 136 stay high relative to the node 150. In the reverse situation, the voltage at node 150 should rise and the voltage at node 136

should drop. However, the transistor 148 tends to preserve the voltage at node 136 until it is overcome.

It will be seen from the above that the CMOS substrate bias generator illustrated provides an on-chip voltage of −2.5 volts from a power supply of +5 volts. The circuitry according to the preferred embodiment includes a nine stage ring oscillator, logic gates, a charge pump and a voltage regulator, which generate a substrate bias in an efficient manner with a low transistor count.

It will be seen that only P channel transistors are used in the charge pump so that no electron injection will take place from nodes which swing to a negative voltage. Additionally, as the power supply is ramped up, the circuit starts to pump when VCC reaches a level which is close to twice the P channel threshold, thus helping to prevent latch-up. CMOS circuits have previously controlled latch-up by grounding the N channel substrate which has detrimental effect on speed. The circuit of the preferred embodiment of this invention does not suffer from this disadvantage.

The regulator circuit illustrated herein maintains the substrate bias at substantially −VCC/2 in a manner which eliminates first order dependence on process parameters. Substrate bias generators which do not use CMOS circuitry have produced voltages which follow threshold variations. In this embodiment, the regulator design sets the substrate to a level of −VCC/2 independent of any Vtn or other process parameters. This gives a better yield.

The circuits described herein can be used advantageously for biasing a P substrate negative in an N well CMOS design or biasing P wells negative in a P well CMOS design. By exchanging N type and P type devices in the circuits, this generator can be used to bias an N substrate positive in a P well CMOS design, or to bias the N wells positive in an N well CMOS design.

It will be understood that a variety of modifications to the embodiment disclosed herein can be made within the scope of the present invention. For example, the timing can be adjusted. The illustrative embodiment uses a 50% duty cycle on waveform V14. A different duty cycle can be used by increasing the number of stages in the ring oscillator to give added delay to the time for which the transistor 20 or the transistor 42 is ON.

CLAIMS

1. A CMOS substrate bias generator comprising a generator circuit for developing a substrate bias voltage, and a regulator for controlling the operation of said generator circuit, said regulator including an input circuit coupled to receive a VBB signal representative of the substrate bias voltage, a reference circuit providing a reference voltage, a comparison circuit coupled to said input circuit and to said reference circuit for comparing voltage levels therein, and output means responsively coupled to said comparison circuit for providing a signal to said generator circuit.

2. A substrate bias generator as claimed in Claim 1, wherein said input circuit is arranged to develop a voltage at a first node by gating a transistor with said VBB signal to regulate current flow from a voltage source to ground, and wherein said reference circuit includes a voltage divider coupled to receive an input from said voltage source.

3. A substrate bias generator as claimed in Claim 1 or 2, wherein said comparison circuit includes hysteresis circuitry tending to preserve voltage at a node in said comparison circuit despite an imbalance between the signals applied thereto.

4. A substrate bias generator as claimed in any of Claims 1 to 3, wherein said generator circuit includes a CMOS charge pump.

5. A CMOS substrate bias generator as claimed in any of Claims 1 to 4, wherein said generator circuit is a substrate bias generator as claimed in any of Claims 1 to 15.

6. A substrate bias generator substantially as hereinbefore described with reference to the accompanying drawings.

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